REMARKS

Claims 1, 3, 4, 6, and 20-26 were pending. Claims 1, 20 and 24 were amended. Claims 27-29 are new. Claims 1, 3, 4, 6, and 20-29 now are pending. (14 claims total, of which claims 1 and 27 are independent).

I. 35 USC 112(2): Claims 20 and 24

The Examiner rejected claims 20 and 24 under 35 USC 112(2) as including indefinite language. The Examiner requests an explanation as to what is meant by "graph base layers" and by "first and second epitaxial thickness."

While looking at Figure 5, a base layer 132 may be viewed as disposed between a left graft base layer 133 and a right graft base layer 133. Graft base layer 133 may be thought of as one graft base layer having two parts, or as two graft base layers. Moreover, graft base layer 133 of Figure 5 may be thought of as areas that particularly isolate an emitter layer 134 by being "grafted" onto a base layer 132. Similarly, graft base layer 153 of Figure 5 may be thought of as areas that particularly isolate an emitter layer 154 by being "grafted" onto a base layer 132. The specification discussions related to Figure 8O and Figure 8P and to Figure 12H and Figure 12I explain examples of this.

Disposed between the lower surface of base layer 132 of Figure 5 and the upper surface of the first embedded diffusion layer 131 is an epitaxial layer 112. The thickness of epitaxial layer 112 at this location may represent a "first epitaxial thickness" (or a "thin collector layer" -- Specification at page 21, line 18). The epitaxial layer 112 is also disposed between the lower surface of base layer 152 of Figure 5 and the upper surface of second embedded diffusion layer 151. The thickness of epitaxial layer 112 at this location may represent a "second epitaxial thickness" (or a "thick collector layer" -- Specification at page 21, line 22 and page 21, line 25 to page 22, line 1).

The (i) difference between the first epitaxial thickness and the second epitaxial thickness plus (ii) the differences between the impurity concentrations of the first embedded diffusion layer 131 and the second embedded diffusion layer 151 (see Specification Figures 6 & 7) plus (iii) the differences between the impurity concentrations of the second embedded diffusion layer 151 and the epitaxial layer 112 at the second epitaxial thickness (See Figure 7) plus (iv) the positioning between the first embedded diffusion layer 131 upper surface and the second embedded diffusion layer 151 upper surface relative to the datum surface of substrate 111, plus (v) the positioning between the base layer 132 lower surface and the base layer 152 lower surface relative to the datum surface of substrate 111, may each contribute to making transistor 101 a high speed transistor and transistor 102 a high voltage transistor all on a single substrate 111. As a "high" voltage transistor, the second vertical type bipolar transistor 102 may have a breakdown voltage that is higher than a breakdown voltage of the first vertical type bipolar transistor 101.

Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection to the claims.

II. 35 USC 103(a)

A. Claims 1, 3, 4, 6, 20-21 and 23-26

The Examiner rejected claims 1, 3, 4, 6, 20-21 and 23-26 under 35 USC 103(a) as unpatentable over Kumamaru (U.S. 4,379,726) or Watanabe (U.S. 4,258,379).

Applicant disagrees that a combination using either Kumamaru or Watanabe teaches each subject matter in the claims.

a. Kumamaru

Claim 1 recites:

a second embedded diffusion layer formed directly on the substrate

The Examiner presents Figure 10 as teaching the claimed semiconductor device. The Examiner presents substrate 1 and epitaxial layer 5 of Kumamaru Figure 10 as teaching the recited substrate 1,5. However, the Examiner presents element region 13 (Figure 8) of Kumamaru as teaching the second embedded diffusion layer. Since the Examiner has failed to provide a motivation to combine the teachings of Figure 8 and Figure 10, the Examiner has failed to make out a prima facie case of 103 obviousness. Moreover, since Figure 8 represents a process step that leads to the semiconductor device of Figure 10, the semiconductor device of Figure 10 can only come into existence if the semiconductor device of Figure 8 is no longer in existence. Accordingly, one would not be motivated to combine the teachings of Figure 8 and the teachings of Figure 10 to construct the claimed semiconductor device.

As noted above, the Examiner presents substrate 1 and epitaxial layer 5 of Kumamaru Figure 10 as teaching the recited substrate 1,5. However, the Examiner relies on the substrate 1, 5 (Figure 8) for the above subject matter. Since the substrate 1, 5 (Figure 8) cannot exist if the substrate 1, 5 (Figure 10) exists, the Examiner has failed to make out a prima facie case of 103 obviousness.

Kumamaru col. 3, lines 24-25 teaches that element region 13 (Figure 8) occupies a portion of layer 5 and a portion of layer 11. Element region 13 (Figure 8) is formed as a result of the conversion of layer 5 (Figure 7) into layer 5a (Figure 8). Occupying a portion of layer 5 and a portion of layer 11 does not teach forming element region 13 directly on the substrate 1, 5. Moreover, converting the substrate 5 into element region 13 does not teach forming element region 13 directly on the substrate 1, 5. Nowhere does Kumamaru teach that element region 13 (Figure 8) is formed directly on the substrate 1, 5 (Figure 10). Kumamaru even fails to teach that element region 13 (Figure 8) is formed directly on the substrate 1, 5 (Figure 8), which appears to be the point that the Examiner is attempting to make.

Claim 1 recites:

a second embedded diffusion layer formed ... within a lower part of the epitaxial layer.

The Examiner presents substrate 1 and epitaxial layer 5 of Kumamaru Figure 10 as teaching the recited substrate 1, 5. The Examiner presents epitaxial layer 11 (Figure 10) as teaching the recited epitaxial layer. The Examiner presents element region 13 (Figure 8) as teaching the second embedded diffusion layer.

The Examiner admits that Kumamaru does not depict second embedded diffusion layer 13 (Figure 8) as being formed within a lower part of the epitaxial layer 11 (Figure 10) or even the epitaxial layer 11 (Figure 8). Here, the Examiner states that Kumamaru's teaching at col. 3, lines 23-26 of forming element region 13 (Figure 8) into a lower part of epitaxial layer 5 (Figure 8) makes the above limitation obvious.

The Examiner has not provided any motivation to combine Kumamaru's teaching of forming element region 13 (Figure 8) into a lower part of epitaxial layer 5 (Figure 8) into Kumamaru's teaching of epitaxial layer 11 (Figure 10) and substrate 1, 5 (Figure 10). Moreover, a skilled person would not view Kumamaru element 5 (Figure 8) and Kumamaru element 5 (Figure 10) as two distinct structural pieces since they are the same element. Further, the resulting combination of Kumamaru Figure 8 plus Kumamaru Figure 10 could not exist in fact since Kumamaru Figure 8 is consumed in use to create Kumamaru Figure 10. In Applicant's view, the Examiner is building a house of cards by removing one card from the bottom of the house to place that card on the top of the structure, the result of which can only lead to the collapse of this house of cards.

Claim 1 recites:

wherein the second embedded diffusion layer ... includes an impurity concentration that is less than the impurity concentration of the first embedded diffusion layer.

The Examiner presents Kumamaru buried layer 14 (Figure 10) as teaching the first embedded diffusion layer. Layer 14 (Figure 8) is formed from the upward diffusion of arsenic from region 8 (Figure 8) into layer 11 (Figure 8). Kumamaru does not have, nor has the Examiner cited, any teaching or suggestion with respect to the impurity concentration of layer 14.

The Examiner presents element region 13 (Figure 8) as teaching the second embedded diffusion layer. Kumamaru col. 3, lines 24-25 teaches that element region 13 (Figure 8) is formed as a result of heating the device to 1,200 deg. C to diffuse layer 10 (Figure 7) down into layer 5 (Figure 8) and, presumably, up into layer 11 (Figure 8) so as to occupy a portion of layer 5 and a portion of layer 11. Kumamaru does not have, nor has the Examiner cited, any teaching or suggestion with respect to the impurity concentration of element region 13.

Since Kumamaru does not have any teaching or suggestion with respect to the impurity concentration of layer 14 or the impurity concentration of element region 13, Kumamaru does not teach or even suggest the above limitation.

Claim 1 recites:

wherein the second embedded diffusion layer includes an impurity concentration that ... is equal to or higher than that of the epitaxial layer

The Examiner presents Kumamaru epitaxial layer 11 (Figure 10) as teaching the recited epitaxial layer. Kumamaru teaches that the impurity concentration of epitaxial layer 11 (Figure 10) is $1 \times 10^{14} / cm^3$ to $5 \times 10^{14} / cm^3$. (Kumamaru col. 4, lines 21-25)

The Examiner presents element region 13 (Figure 8) as teaching the second embedded diffusion layer. Kumamaru col. 3, lines 24-25 teaches that element region 13 (Figure 8) is formed as a result of heating the device to 1,200 deg. C to diffuse layer 10 (Figure 7) down into layer 5 (Figure 8) and, presumably, up into layer 11 (Figure 8) so as to occupy a portion

of layer 5 and a portion of layer 11. Kumamaru does not have, nor has the Examiner cited, any teaching or suggestion with respect to the impurity concentration of element region 13.

Kumamaru col. 4, lines 18-20 teaches that the impurity concentration of layer 10 is 1 x 10^{11} / cm^2 to 1.2 x 10^{12} / cm^2. Since the impurity concentration units of layer 11 is / cm^3 and the impurity concentration units of layer 10 is / cm^2, the impurity concentration of these two layers cannot be compared. Even assuming that they can be compared, since the impurity concentration of layer 10 is less than the impurity concentration of layer 11, the impurity concentration of the second embedded diffusion layer 13 is less than the impurity concentration of the epitaxial layer 11. Thus, Kumamaru does not teach the above limitation.

Claim 1 recites

wherein a peak position of an impurity concentration of the first embedded diffusion layer resides at a first distance from the datum surface of the substrate and a peak position of an impurity concentration of the second embedded diffusion layer resides at a second distance from the datum surface of the substrate such that the first distance is greater than the second distance.

The Examiner presents Kumamaru buried layer 14 (Figure 10) as teaching the first embedded diffusion layer. Layer 14 (Figure 8) is formed from the upward diffusion of arsenic from region 8 (Figure 8) into layer 11 (Figure 8). Kumamaru does not have, nor has the Examiner cited, any teaching or suggestion with respect to the impurity concentration of layer 14.

The Examiner presents element region 13 (Figure 8) as teaching the second embedded diffusion layer. Kumamaru col. 3, lines 24-25 teaches that element region 13 (Figure 8) is formed as a result of heating the device to 1,200 deg. C to diffuse layer 10 (Figure 7) down into layer 5 (Figure 8) and, presumably, up into layer 11 (Figure 8) so as to occupy a portion

of layer 5 and a portion of layer 11. Kumamaru does not have, nor has the Examiner cited, any teaching or suggestion with respect to the impurity concentration of element region 13.

In addition to the above, the location of element region 13 (Figure 8) is not clear such that no conclusion can be drawn to the relative peak impurity concentrations. Moreover, the Examiner has not even cited a basis for asserting that either element region 13 or buried layer 14 has a peak impurity concentration. Further, without providing a motivation for the proposed combination, it is the features of element region 13 (Figure 10) that must be compared to the features of buried layer 14 (Figure 10).

For the above reasons, Kumamaru does not teach the above subject matter.

b. Watanabe

Claim 1 preamble recites:

A semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor having a breakdown voltage that is higher than a breakdown voltage of the first vertical type bipolar transistor

Watanabe discloses a semiconductor device having an NPN bipolar transistor 101 and an IIL (Integrated Injection Logic) device 201. However, Watanabe never discloses a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor having a breakdown voltage that is higher than a breakdown voltage of the first vertical type bipolar transistor.

The upper 22" portion is formed in element 41' and element 3 at a close position to base region 52. Accordingly, even if the lower 22" portion formed below element 41' exists in the IIL device 201, the breakdown voltage of the IIL device 201 is determined by the upper 22" portion due to the proximity of the upper 22" portion to the base region 52. Since the upper 22" portion is formed in element 41' and element 3 at a close position to base region 52, the breakdown voltage of the IIL device 201 is lower than that of the NPN bipolar transistor

101, whose distance between base region 53 and first embedded diffusion layer 21 is greater than the distance between base region 52 and the second embedded diffusion layer 22". Therefore, Watanabe never discloses "a first vertical type bipolar transistor and a second vertical type bipolar transistor having a breakdown voltage that is higher than a breakdown voltage of the first vertical type bipolar transistor" as recited in claim 1.

Claim 1 recites:

wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer

The Examiner presents element 21 (Figure 8) of Watanabe as teaching the first embedded diffusion layer and element 22" (Figure 8) of Watanabe as teaching the second embedded diffusion layer. Both Figure 8 and Figure 9 of Watanabe clearly shows that first embedded diffusion layer 21 is disposed within the second embedded diffusion layer 22". Thus, Watanabe does not teach the above subject matter. Watanabe teaches disposing the first embedded diffusion layer 21 within the second embedded diffusion layer 22" to achieve a sufficient high breakdown voltage. (Watanabe col. 6, lines 18-28; col. 9, lines 31-33 and lines 51-53) Thus, one would not be motivated to modify the teachings of Watanabe in this regard.

c. Conclusion

For the above reasons, Applicant respectfully requests that the Examiner withdraw the rejection to the claims.

B. Claim 22

The Examiner rejected claim 22 under 35 USC 103(a) as unpatentable over Kumamaru (U.S. 4,379,726) or Watanabe (U.S. 4,258,379) in view of Admitted Prior Art.

Claim 22 depends on claim 1.

For the above reasons, Applicant respectfully requests that the Examiner withdraw the rejection to the claim.

III. New claims 27-29

New claims 27-29 are not taught by the cited art. For example,

claim 27 recites:

wherein only the epitaxial layer is disposed between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer

Kumamaru (U.S. 4,379,726) Figure 8 shows layer 41' is disposed between diffusion layer 22" and the lower surface of the base layer 52. Kumamaru states that the integrated injection logic device of the Kumamaru will not work if buried layer 21" (e.g., buried layer 21' with a different shape, Kumamaru col. 9, lines 31-33) is used separate from well 41'. (Kumamaru col. 7, lines 15-21) Watanabe (U.S. 4,258,379) does not teach the subject matter of claim 27-29 for the reasons stated above. Thus, neither cited art teaches the subject matter of claims 27-29.

IV. Conclusion

In view of the foregoing, it is believed that the claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
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Dated: October 2, 2001

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Rose M. Garza Date: October 2, 2001

V. APPENDIX TO RESPONSE "I" TO NON FINAL OFFICE ACTION: VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

1. (Amended Seven Times) A semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor having a breakdown voltage that is higher than a breakdown voltage of the first vertical type bipolar transistor, the semiconductor device comprising:

a substrate defining a datum surface, wherein the substrate is a first conductive type substrate;

an epitaxial layer formed on the substrate above the datum surface;

a first embedded diffusion layer formed as part of a first vertical type bipolar transistor in a first upper part of the substrate and in the epitaxial layer;

a second embedded diffusion layer formed as part of a second vertical type bipolar transistor directly on the substrate, in a second upper part of the substrate, and within a lower part of the epitaxial layer,

wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer,

wherein the second embedded diffusion layer is a second conductive type second embedded diffusion layer that is a different conductive type from the first conductive type substrate and includes an impurity concentration that is less than the impurity concentration of the first embedded diffusion layer and is equal to or higher than that of the epitaxial layer, and

wherein a peak position of an impurity concentration of the first embedded diffusion layer resides at a first distance from the datum surface of the substrate and a peak position of an impurity concentration of the second embedded diffusion layer resides at a second distance

from the datum surface of the substrate such that the first distance is greater than the second distance.

20. (Amended Three Times) A semiconductor device according to claim 1, further comprising:

a first base layer disposed between two first graft base layers and disposed above the first embedded diffusion layer on the epitaxial layer to define a first epitaxial thickness between the first base layer and the first embedded diffusion layer; and

a second base layer disposed between two second graft base layers and disposed above the second embedded diffusion layer on the epitaxial layer to define a second epitaxial thickness between the second base layer and the second embedded diffusion layer,

wherein the first epitaxial thickness is less than the second epitaxial thickness, and

wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer.

24. (Amended One Time) A semiconductor device according to claim 1, wherein the second vertical type bipolar transistor includes a base layer disposed between two ~~graph~~ graft base layers and wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer.